PAGE	DESCRIPTION	NOTE
1	01_TItle	
2	02_Block	
3	03_BANK0	
4	04_BANK12_13	
5	05_BANK_33_34_35	
6	06_BANK_MGT	
7	07_BANK_PS	
8	08_BANK_PWR	
9	09_DDR_PL	
10	10_DDR_PS	
11	11_PL_DDR_PULLUP	
12	12_PS_DDR_PULLUP	
13	13_QSPI_FLASH	
14	14_SD1_EMMC	
15	15_PMU	
16	16_connect	
17		
18		
19		
20		
21		
22		

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8GB EMMC

256Mbit Flash



PL 1GB DDR3L

PS 1GB DDR3L

1V0内核电源







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ProjectName: <Doc>			
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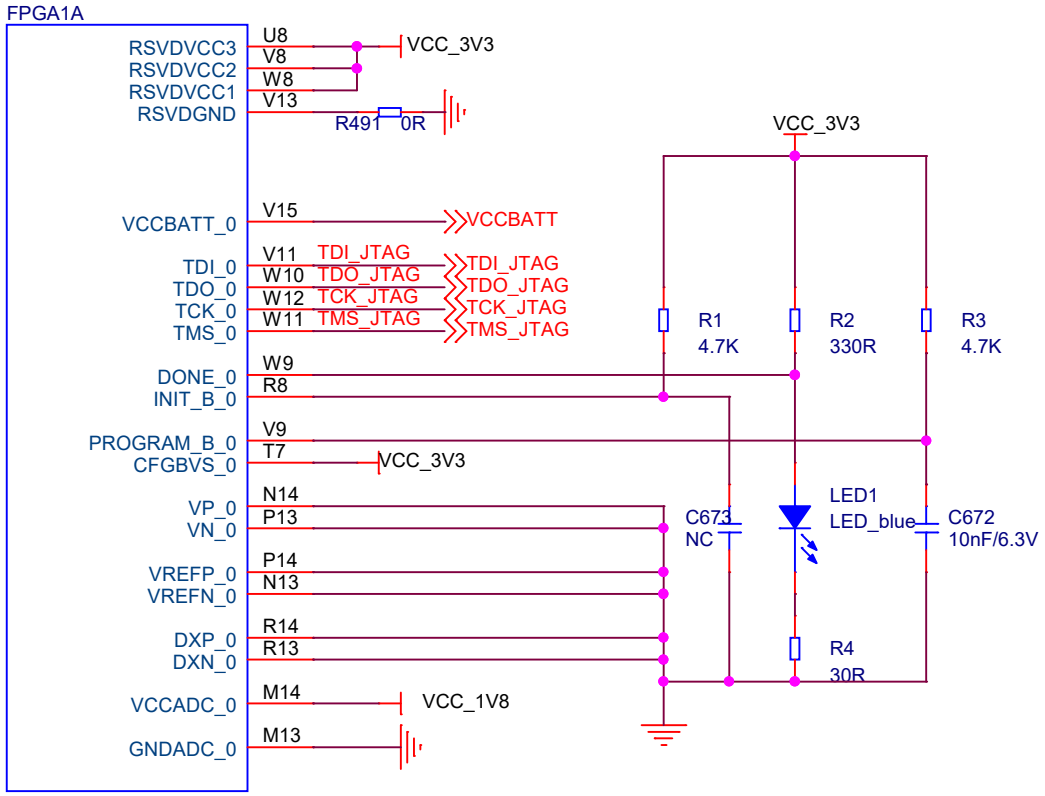

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Size: A	Page Title: 03_BANK0	Rev:	20241205
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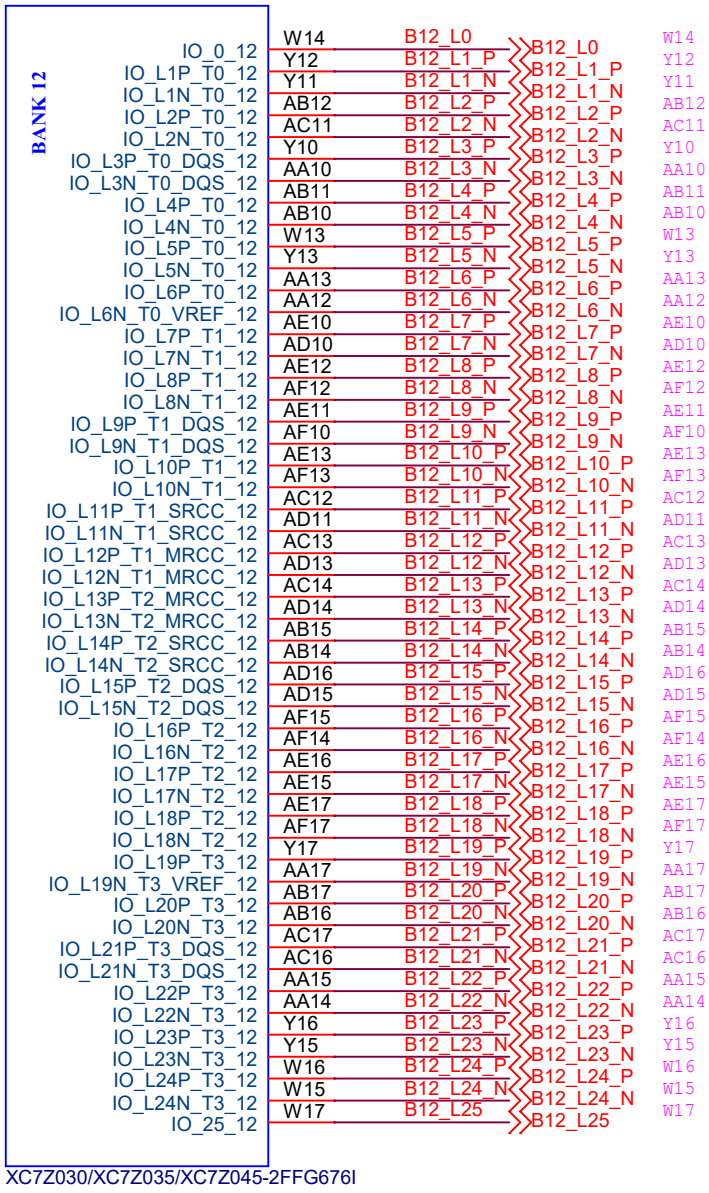
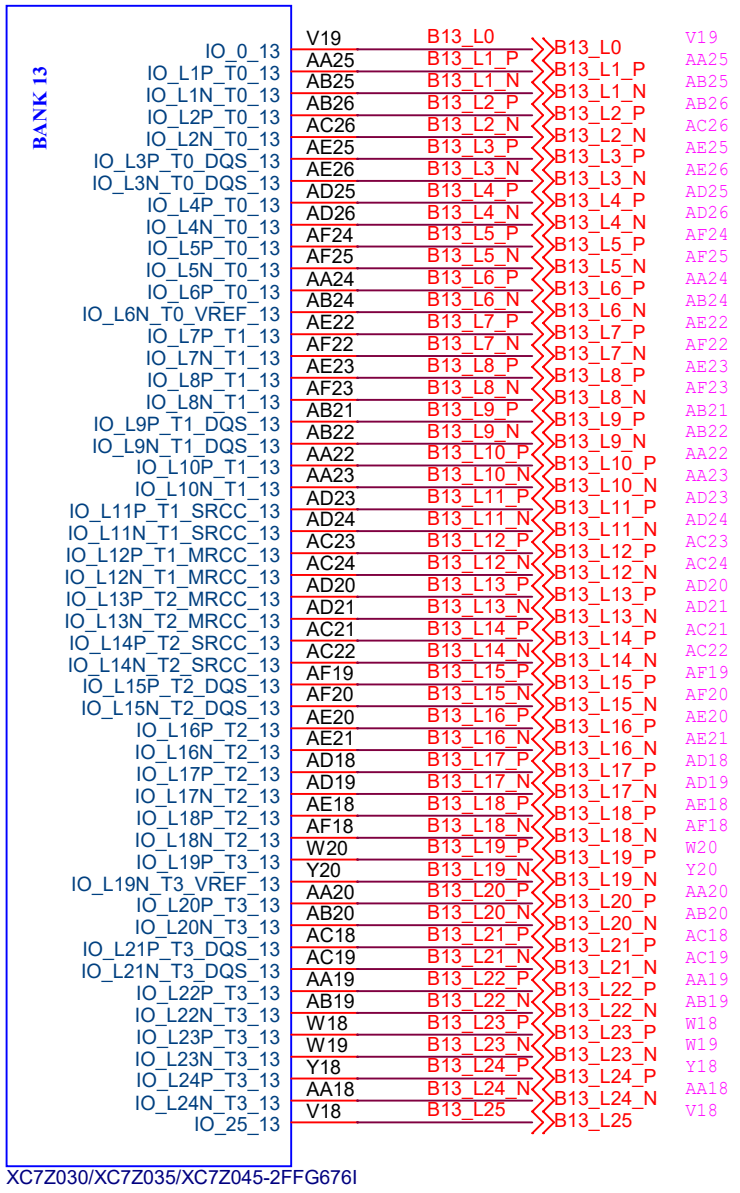
FPGA1B



XC7Z030/XC7Z035/XC7Z045-2FFG676I

FPGA1C



XC7Z030/XC7Z035/XC7Z045-2FFG676I

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ProjectName: <Doc>			
Size: A	Page Title: 04_BANK12_13	Rev:	20241205
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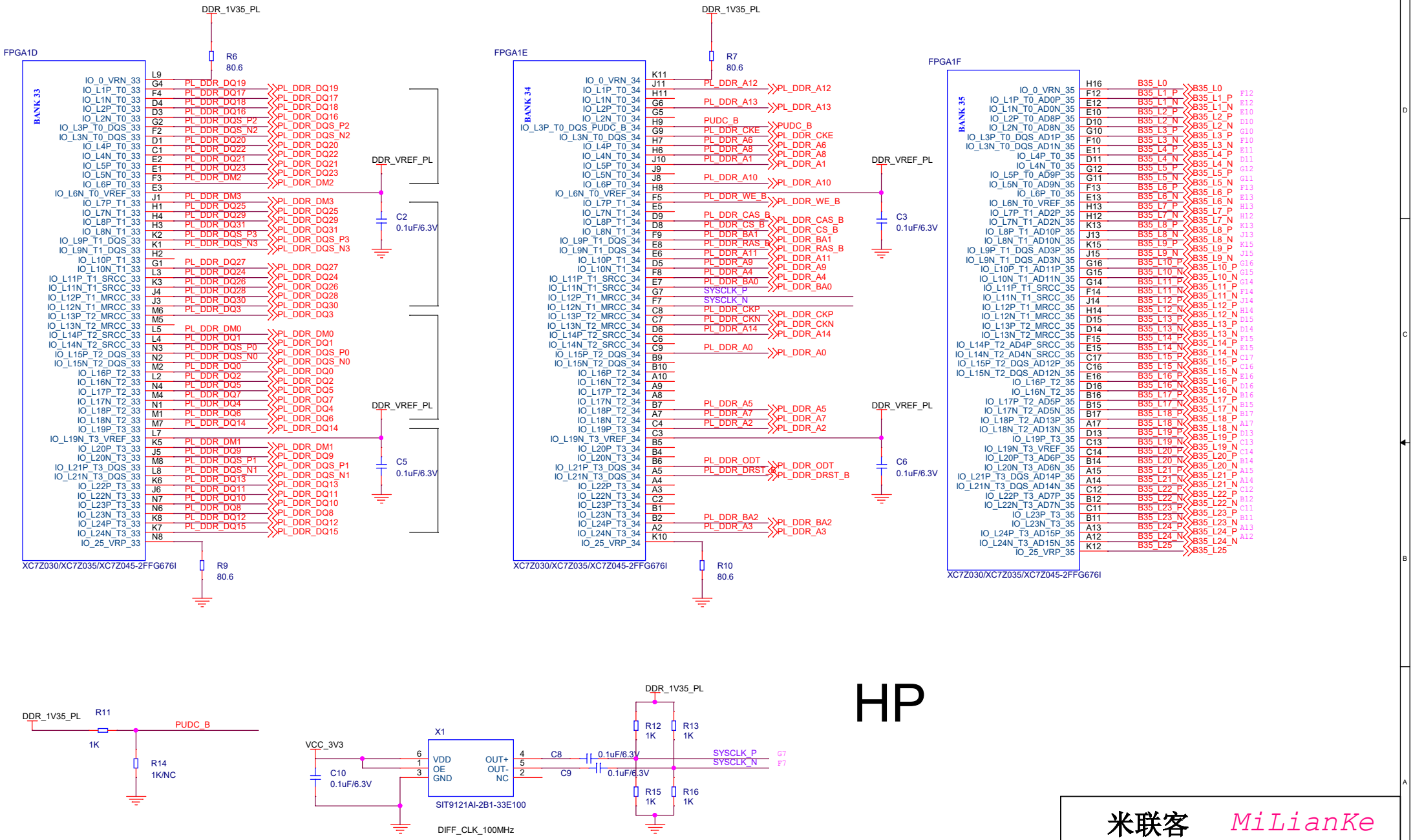
FPGA1D
DDR_1V35_PL
R6
80.6
BANK 33
IO_0_VRN_33
IO_L1P_T0_33
IO_L1N_T0_33
IO_L2P_T0_33
IO_L2N_T0_33
IO_L3P_T0_DQS_33
IO_L3N_T0_DQS_33
IO_L4P_T0_33
IO_L4N_T0_33
IO_L5P_T0_33
IO_L5N_T0_33
IO_L6P_T0_33
IO_L6N_T0_VREF_33
IO_L7P_T1_33
IO_L7N_T1_33
IO_L8P_T1_33
IO_L8N_T1_33
IO_L9P_T1_DQS_33
IO_L9N_T1_DQS_33
IO_L10P_T1_33
IO_L10N_T1_33
IO_L11P_T1_SRCC_33
IO_L11N_T1_SRCC_33
IO_L12P_T1_MRCC_33
IO_L12N_T1_MRCC_33
IO_L13P_T2_MRCC_33
IO_L13N_T2_MRCC_33
IO_L14P_T2_SRCC_33
IO_L14N_T2_SRCC_33
IO_L15P_T2_DQS_33
IO_L15N_T2_DQS_33
IO_L16P_T2_33
IO_L16N_T2_33
IO_L17P_T2_33
IO_L17N_T2_33
IO_L18P_T2_33
IO_L18N_T2_33
IO_L19P_T3_33
IO_L19N_T3_VREF_33
IO_L20P_T3_33
IO_L20N_T3_33
IO_L21P_T3_DQS_33
IO_L21N_T3_DQS_33
IO_L22P_T3_33
IO_L22N_T3_33
IO_L23P_T3_33
IO_L23N_T3_33
IO_L24P_T3_33
IO_L24N_T3_33
IO_25_VRP_33
PL_DDR_DQ19
PL_DDR_DQ17
PL_DDR_DQ18
PL_DDR_DQ16
PL_DDR_DQS_P2
PL_DDR_DQS_N2
PL_DDR_DQ20
PL_DDR_DQ22
PL_DDR_DQ21
PL_DDR_DQ23
PL_DDR_DM2
PL_DDR_DM3
PL_DDR_DQ25
PL_DDR_DQ29
PL_DDR_DQ31
PL_DDR_DQS_P3
PL_DDR_DQS_N3
PL_DDR_DQ27
PL_DDR_DQ24
PL_DDR_DQ26
PL_DDR_DQ28
PL_DDR_DQ30
PL_DDR_DQ3
PL_DDR_DM0
PL_DDR_DQ1
PL_DDR_DQS_P0
PL_DDR_DQS_N0
PL_DDR_DQ0
PL_DDR_DQ2
PL_DDR_DQ5
PL_DDR_DQ7
PL_DDR_DQ4
PL_DDR_DQ6
PL_DDR_DQ14
PL_DDR_DM1
PL_DDR_DQ9
PL_DDR_DQS_P1
PL_DDR_DQS_N1
PL_DDR_DQ13
PL_DDR_DQ11
PL_DDR_DQ10
PL_DDR_DQ8
PL_DDR_DQ12
PL_DDR_DQ15
DDR_VREF_PL
C2
0.1uF/6.3V
C5
0.1uF/6.3V
XC7Z030/XC7Z035/XC7Z045-2FFG676I
R9
80.6
FPGA1E
DDR_1V35_PL
R7
80.6
BANK 34
PL_DDR_A12
PL_DDR_A13
PUDC_B
PL_DDR_CKE
PL_DDR_A6
PL_DDR_A8
PL_DDR_A1
PL_DDR_A10
PL_DDR_WE_B
PL_DDR_CAS_B
PL_DDR_CS_B
PL_DDR_BA1
PL_DDR_RAS_B
PL_DDR_A11
PL_DDR_A9
PL_DDR_A4
PL_DDR_BA0
SYSCLK_P
SYSCLK_N
PL_DDR_CKP
PL_DDR_CKN
PL_DDR_A14
PL_DDR_A0
PL_DDR_A5
PL_DDR_A7
PL_DDR_A2
PL_DDR_ODT
PL_DDR_DRST_B
PL_DDR_BA2
PL_DDR_A3
DDR_VREF_PL
C3
0.1uF/6.3V
C6
0.1uF/6.3V
XC7Z030/XC7Z035/XC7Z045-2FFG676I
R10
80.6
FPGA1F
BANK 35
B35_L0
B35_L1_P
B35_L1_N
B35_L2_P
B35_L2_N
B35_L3_P
B35_L3_N
B35_L4_P
B35_L4_N
B35_L5_P
B35_L5_N
B35_L6_P
B35_L6_N
B35_L7_P
B35_L7_N
B35_L8_P
B35_L8_N
B35_L9_P
B35_L9_N
B35_L10_P
B35_L10_N
B35_L11_P
B35_L11_N
B35_L12_P
B35_L12_N
B35_L13_P
B35_L13_N
B35_L14_P
B35_L14_N
B35_L15_P
B35_L15_N
B35_L16_P
B35_L16_N
B35_L17_P
B35_L17_N
B35_L18_P
B35_L18_N
B35_L19_P
B35_L19_N
B35_L20_P
B35_L20_N
B35_L21_P
B35_L21_N
B35_L22_P
B35_L22_N
B35_L23_P
B35_L23_N
B35_L24_P
B35_L24_N
B35_L25
XC7Z030/XC7Z035/XC7Z045-2FFG676I
DDR_1V35_PL
R11
1K
PUDC_B
R14
1K/NC
VCC_3V3
X1
VDD
OE
GND
OUT+
OUT-
NC
SIT9121AI-2B1-33E100
C10
0.1uF/6.3V
C8
C9
0.1uF/6.3V
0.1uF/6.3V
DIFF_CLK_100MHz
DDR_1V35_PL
R12
1K
R13
1K
R15
1K
R16
1K
SYSCLK_P
SYSCLK_N
HP
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ProjectName: <Doc>
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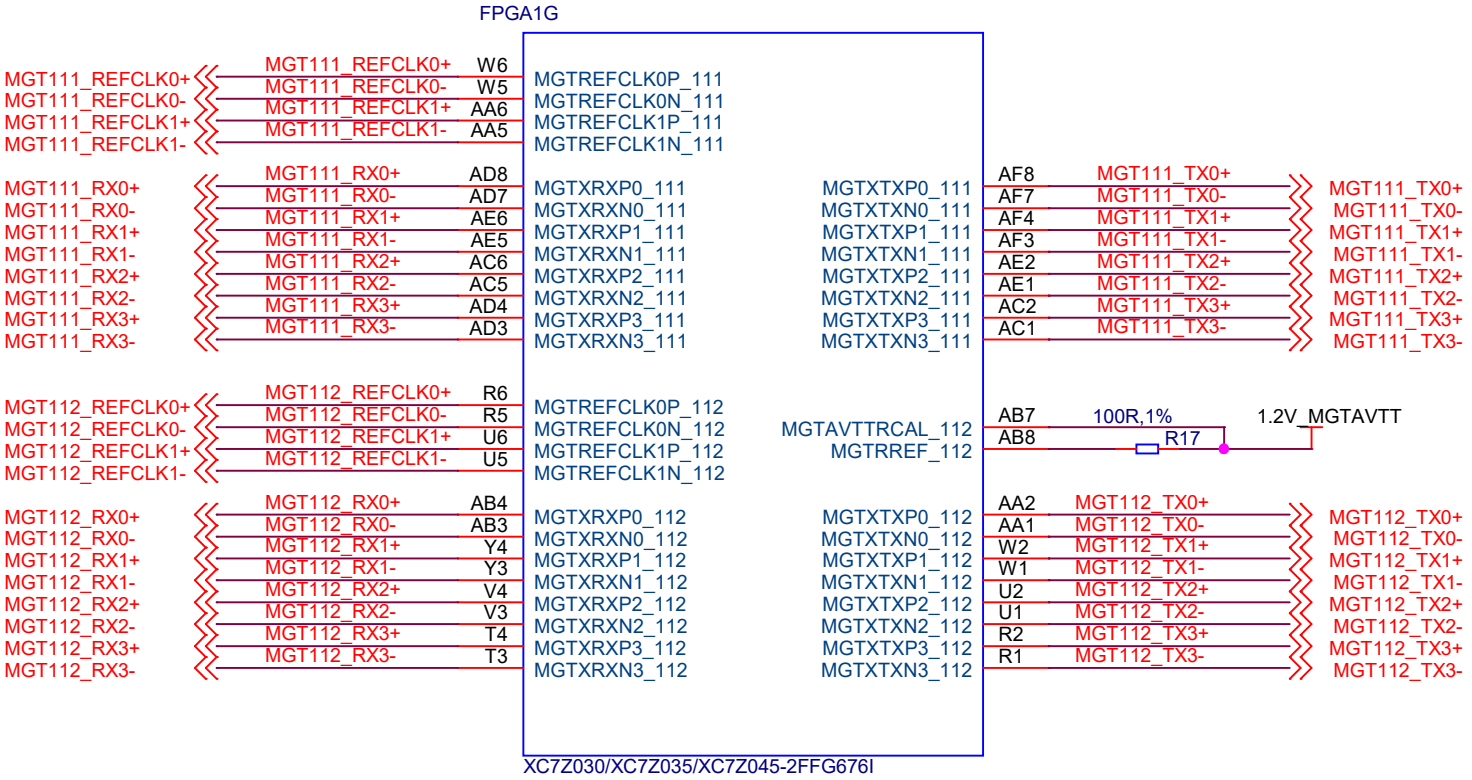

XC7Z030-2FFG676I无MGT111

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ProjectName: <Doc>			
Size: A	Page Title: 06_BANK_MGT	Rev:	20241205
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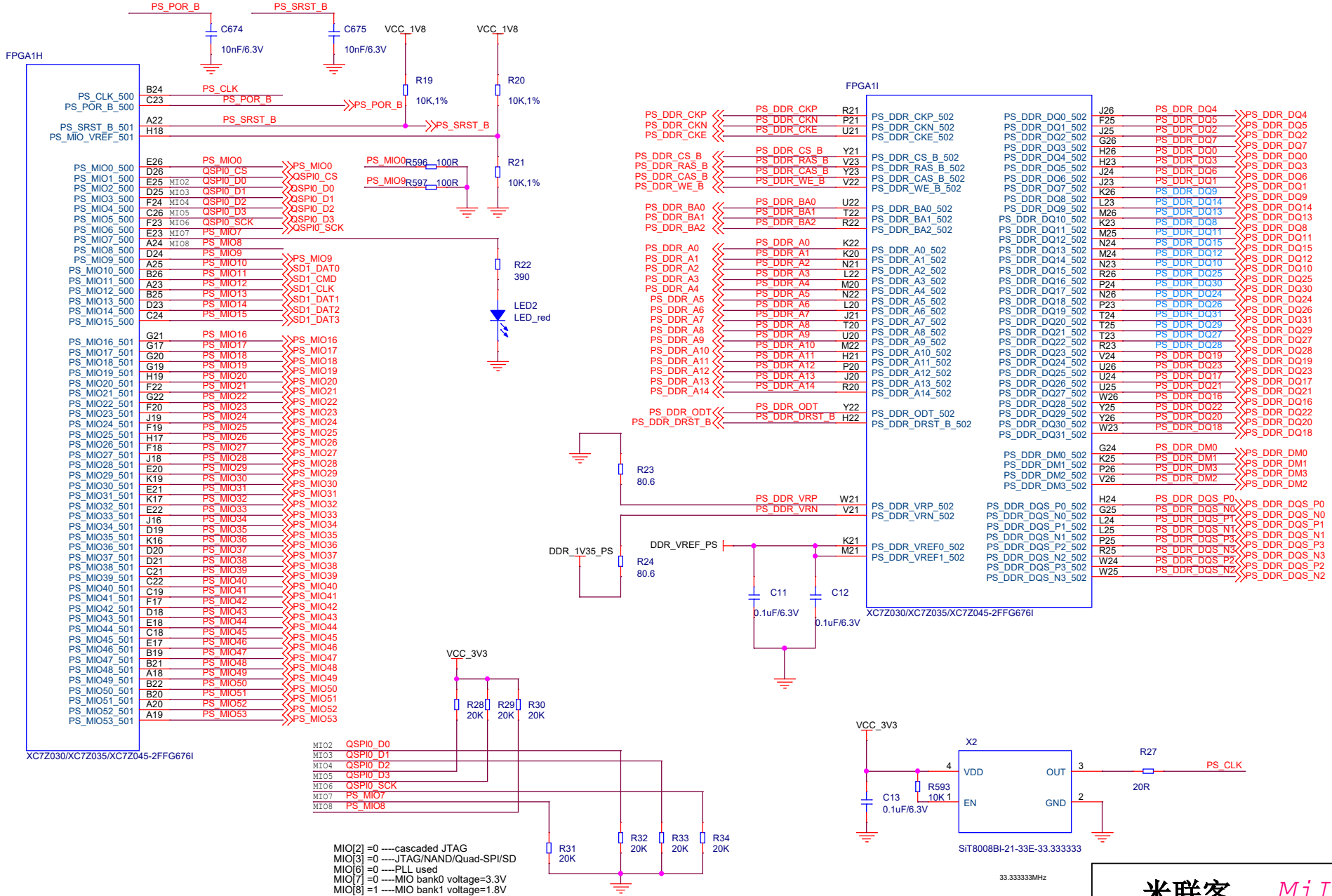
FPGA1H
XC7Z030/XC7Z035/XC7Z045-2FFG676I
PS_POR_B
PS_SRST_B
C674
10nF/6.3V
C675
10nF/6.3V
VCC_1V8
VCC_1V8
R19
10K,1%
R20
10K,1%
R21
10K,1%
R596 100R
R597 100R
R22
390
LED2
LED_red
FPGA1I
XC7Z030/XC7Z035/XC7Z045-2FFG676I
R23
80.6
R24
80.6
DDR_1V35_PS
DDR_VREF_PS
C11
0.1uF/6.3V
C12
0.1uF/6.3V
VCC_3V3
R28 20K
R29 20K
R30 20K
R31 20K
R32 20K
R33 20K
R34 20K
MIO[2] =0 ----cascaded JTAG
MIO[3] =0 ----JTAG/NAND/Quad-SPI/SD
MIO[6] =0 ----PLL used
MIO[7] =0 ----MIO bank0 voltage=3.3V
MIO[8] =1 ----MIO bank1 voltage=1.8V
VCC_3V3
X2
R593 10K 1
C13 0.1uF/6.3V
R27 20R
SiT8008BI-21-33E-33.333333
33.333333MHz
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ProjectName: <Doc>
Size: B
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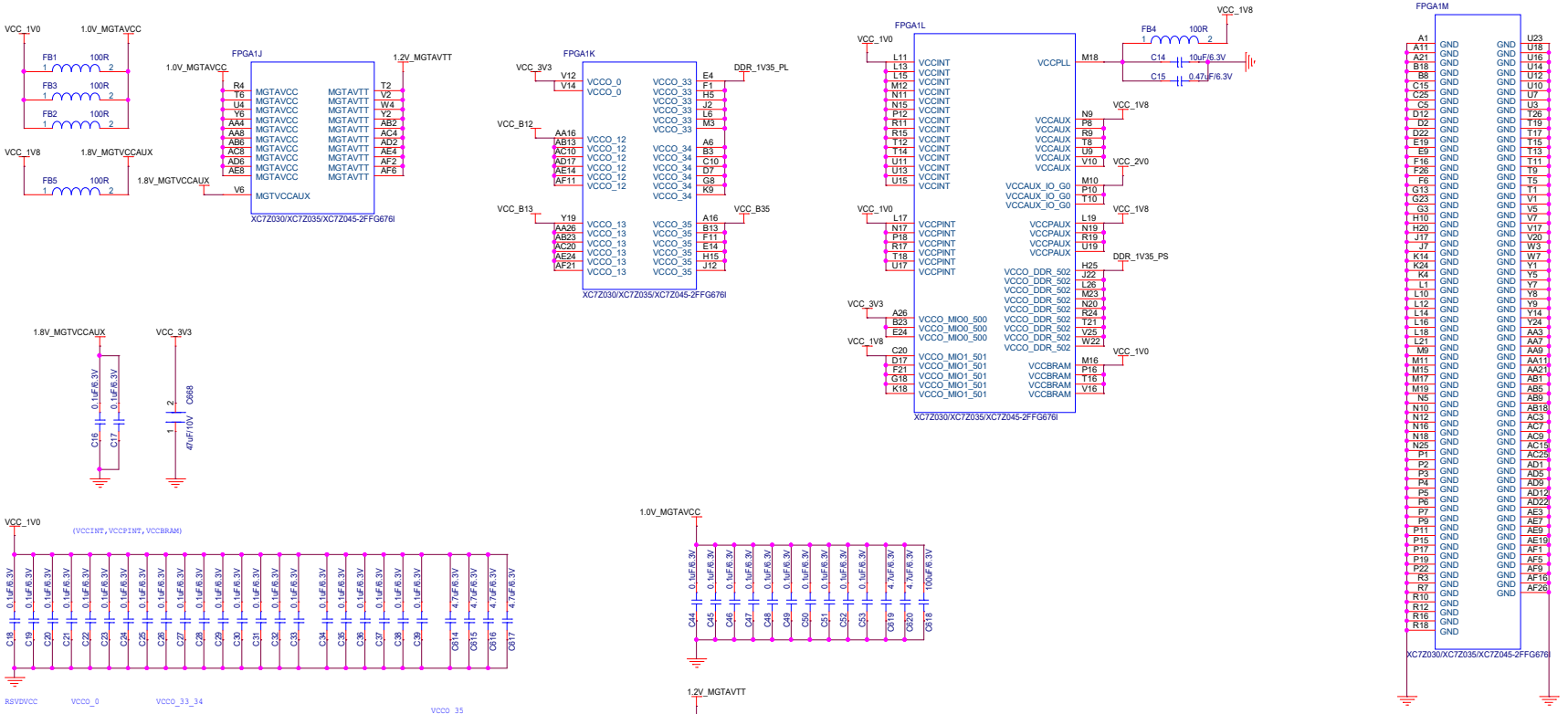

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ProjectName:	<Doc>		
Size: C	Page Title: 08_BANK_PWR	Rev:	20241205
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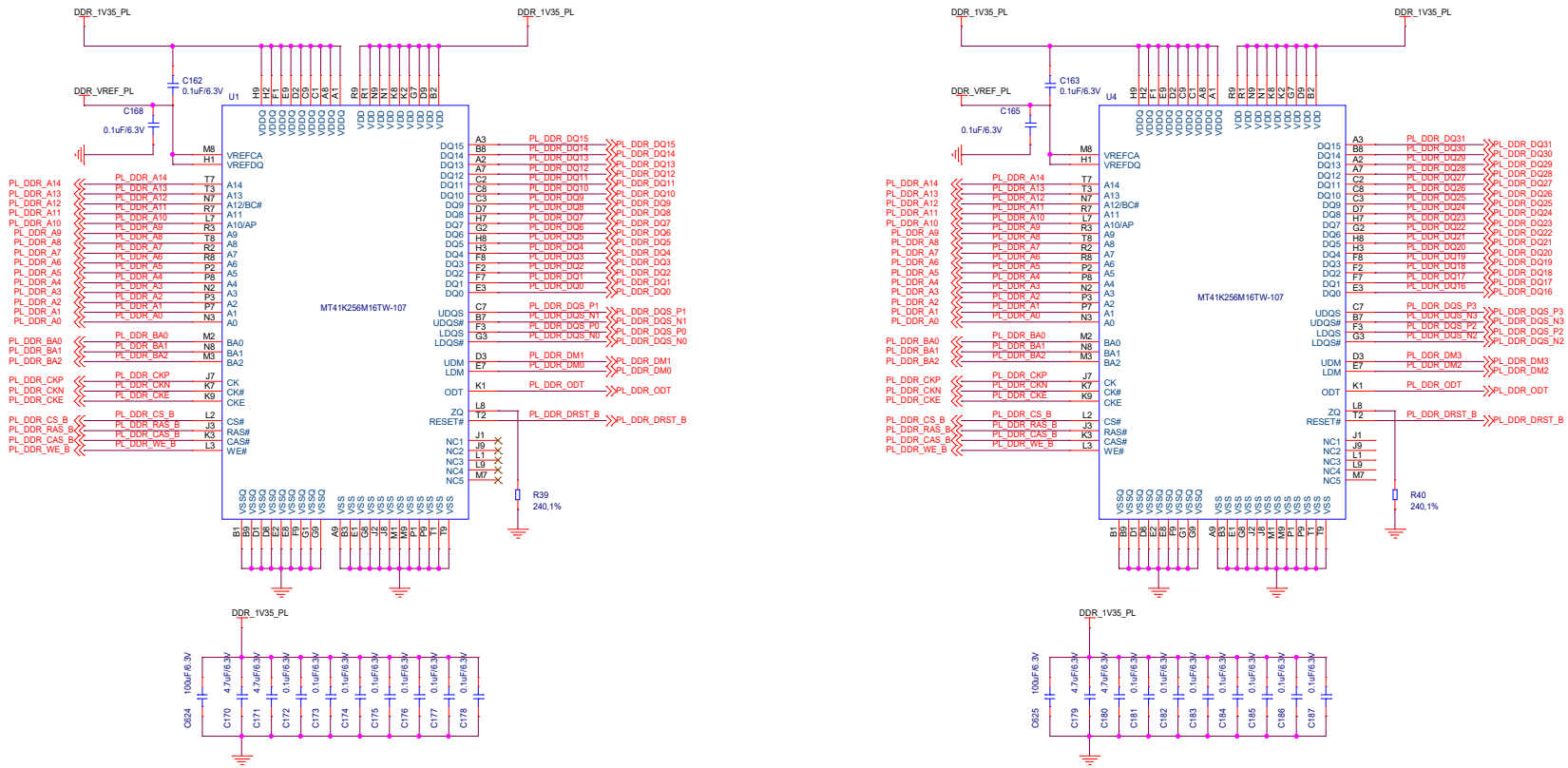

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ProjectName:	<Doc>		
Size: C	Page Title: 09_DDR_PL	Rev:	20241205
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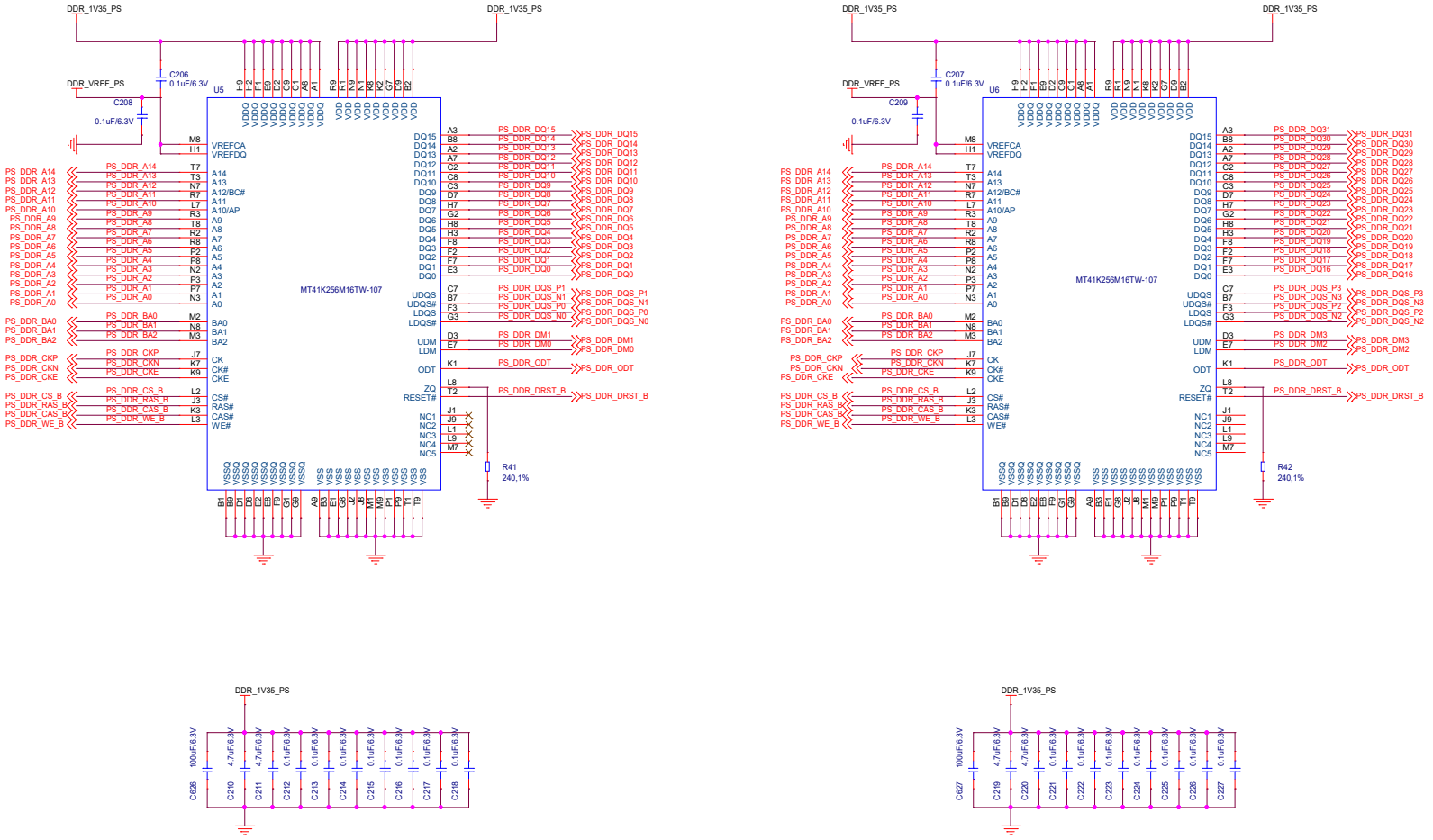
PS_DDR3 X2



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ProjectName:	<Doc>		
Size: C	Page Title: 10_DDR_PS	Rev:	20241205
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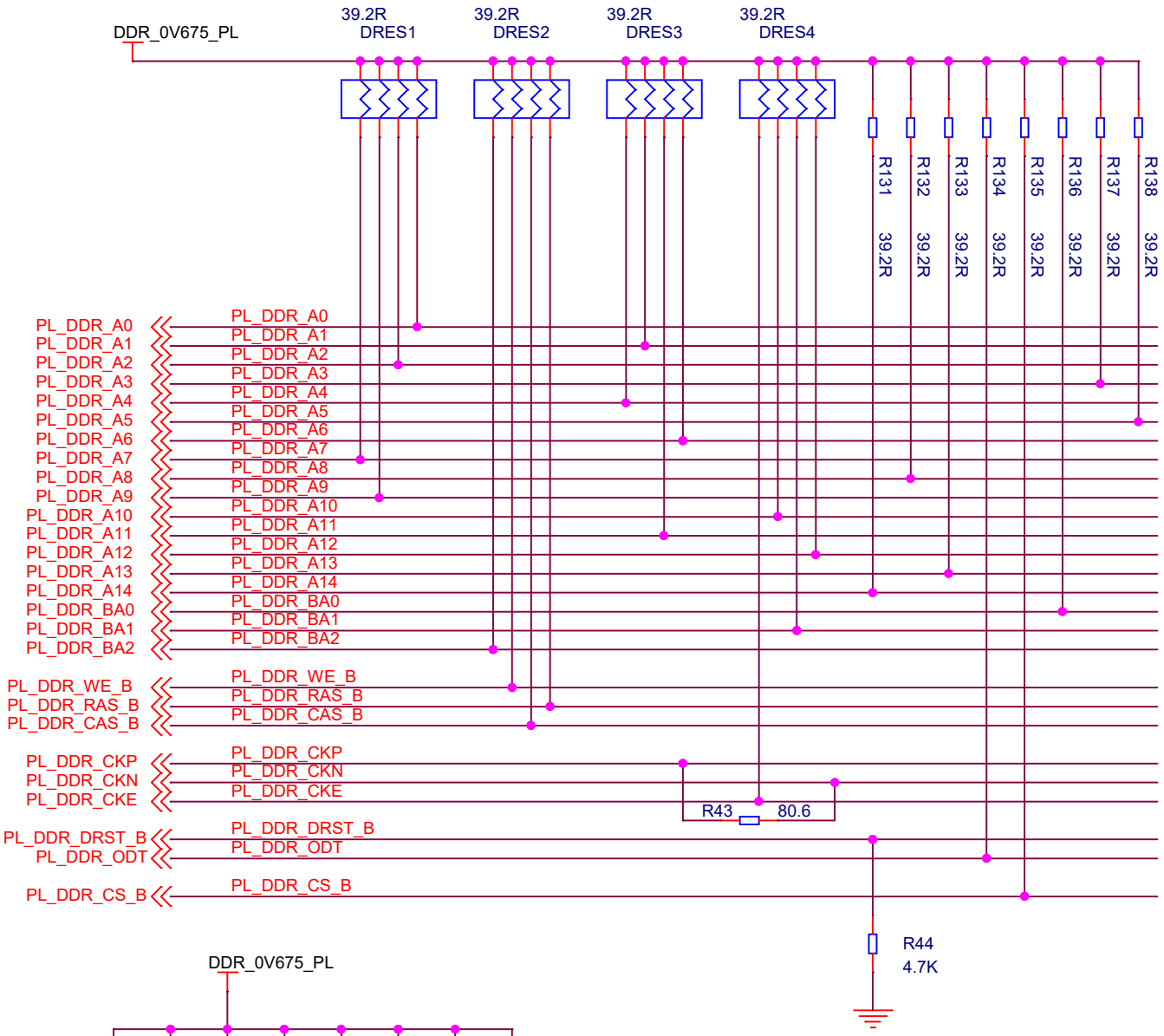

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ProjectName: <Doc>			
Size: A	Page Title: 11_PL_DDR_PULLUP	Rev:	20241205
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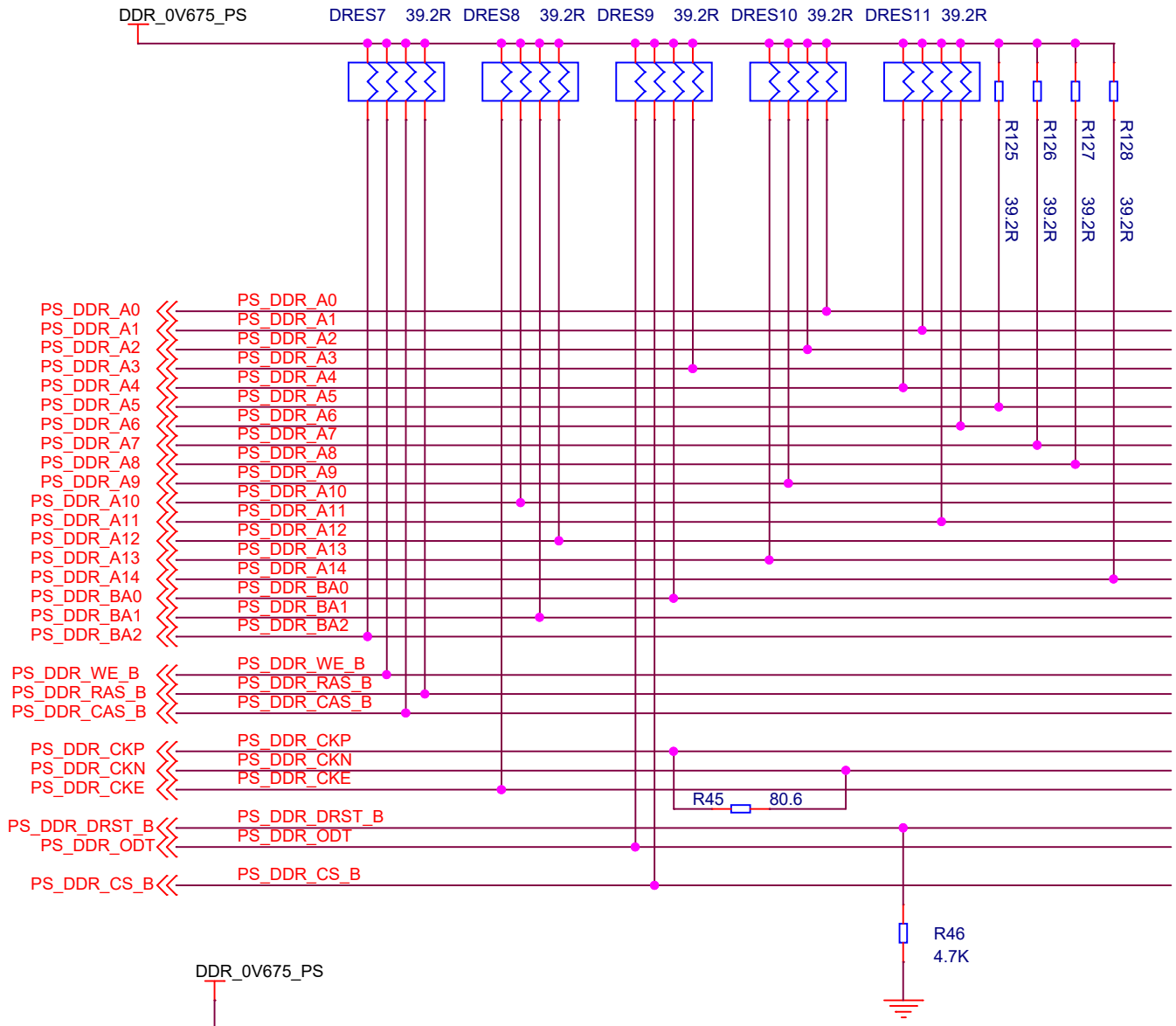

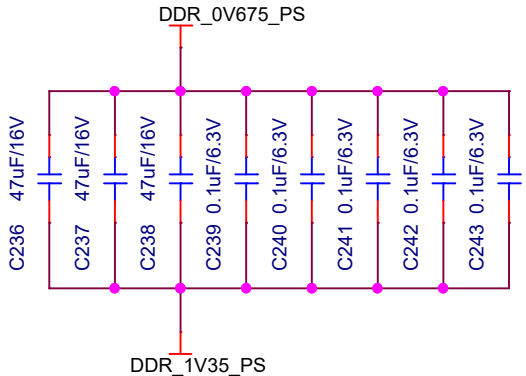

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ProjectName: <Doc>			
Size: A	Page Title: 12_PS_DDR_PULLUP	Rev:	20241205
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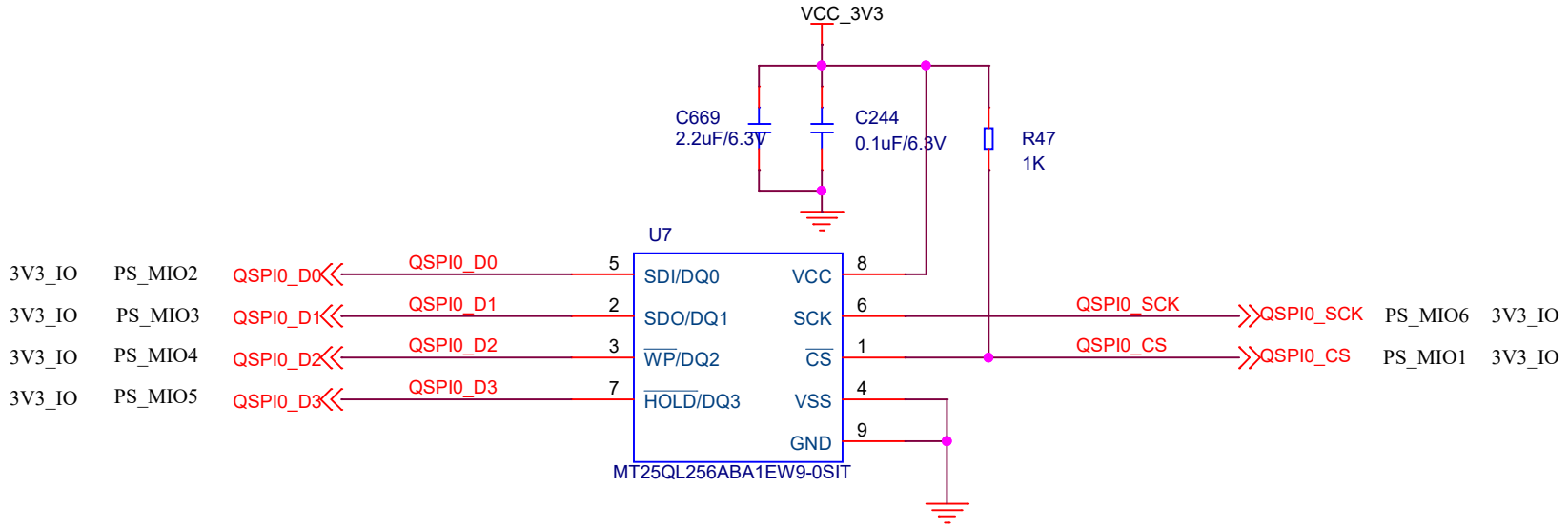

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ProjectName: <Doc>			
Size: A	Page Title: 13_QSPI_FLASH	Rev:	20241205
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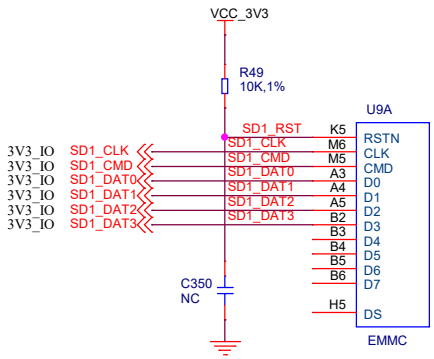
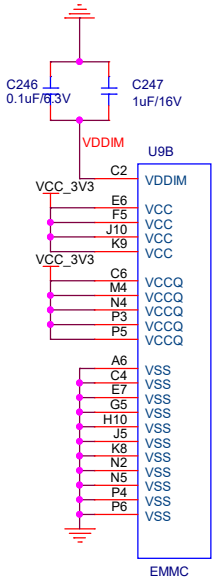
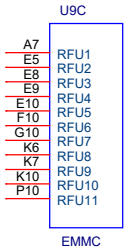
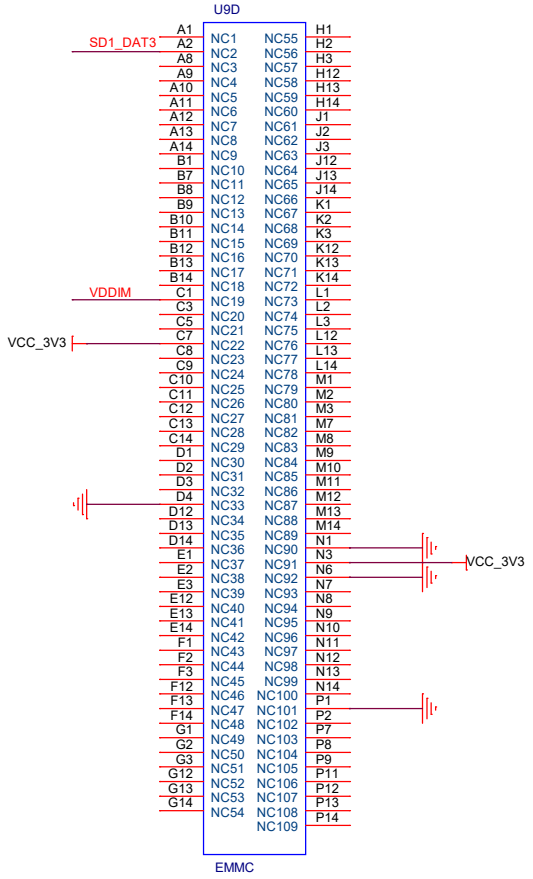
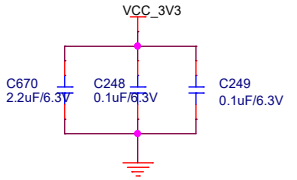


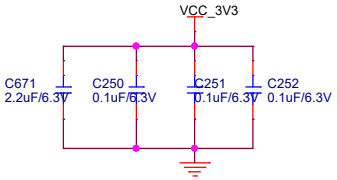
EMMC型号：FEMDRW008G-88A39











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ProjectName: <Doc>			
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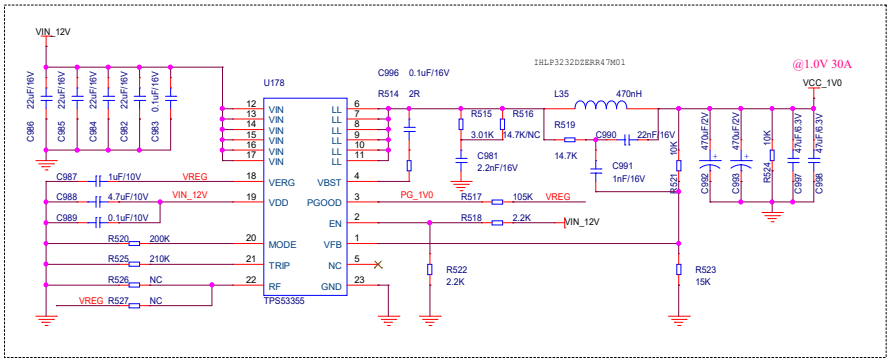
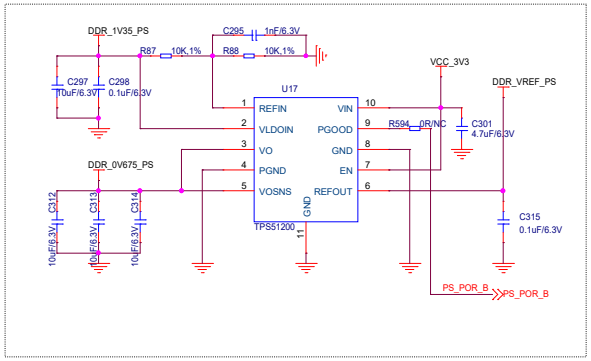
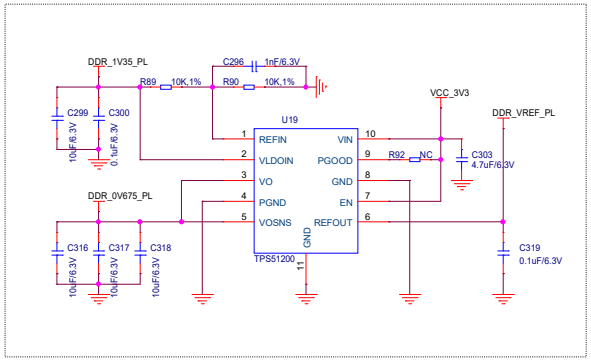
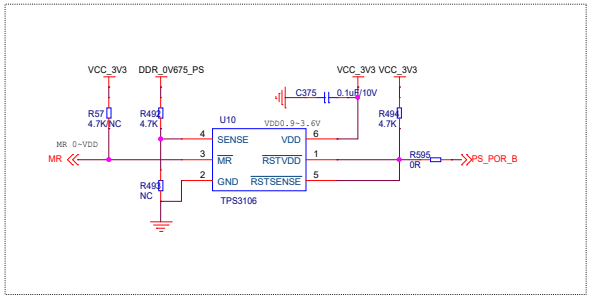
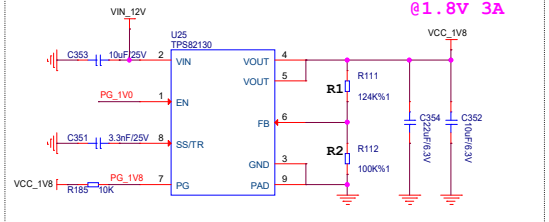








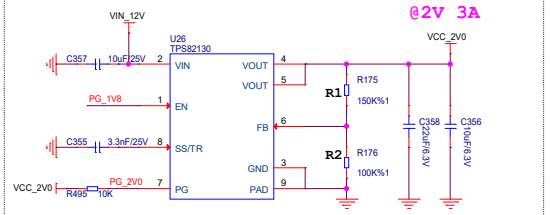
输入电压：3-17V
输出电流：3A
输出电压：0.9-5V



PG：上限上拉电压6V
EN阈值为0.65-0.9V

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.8\ V \times \left(1 + \frac{R1}{R2}\right)$$

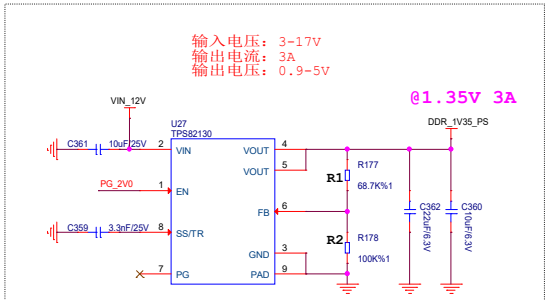
输入电压：3-17V
输出电流：3A
输出电压：0.9-5V



PG：上限上拉电压6V
EN阈值为0.65-0.9V

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.8\ V \times \left(1 + \frac{R1}{R2}\right)$$

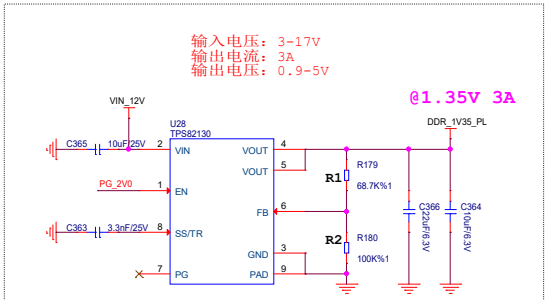
输入电压：3-17V
输出电流：3A
输出电压：0.9-5V



PG：上限上拉电压6V
EN阈值为0.65-0.9V

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.8\ V \times \left(1 + \frac{R1}{R2}\right)$$

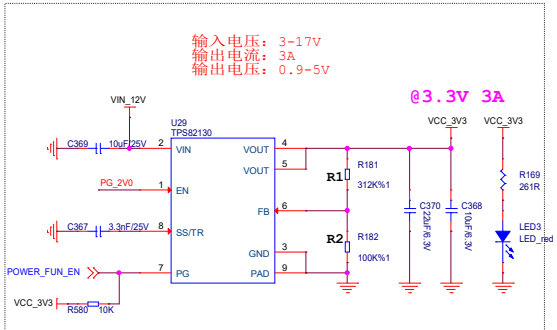
输入电压：3-17V
输出电流：3A
输出电压：0.9-5V



PG：上限上拉电压6V
EN阈值为0.65-0.9V

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.8\ V \times \left(1 + \frac{R1}{R2}\right)$$

输入电压：3-17V
输出电流：3A
输出电压：0.9-5V



PG：上限上拉电压6V
EN阈值为0.65-0.9V

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.8\ V \times \left(1 + \frac{R1}{R2}\right)$$

输入电压：3-17V
输出电流：3A
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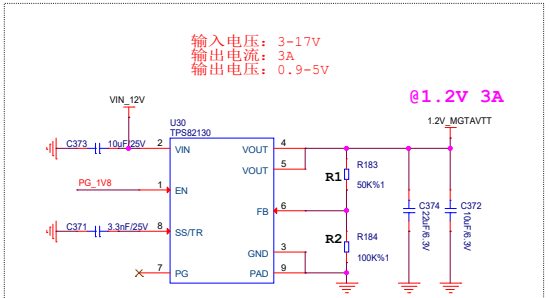

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米联客 MiLianKe
www.milianke.com MLK-CZ10

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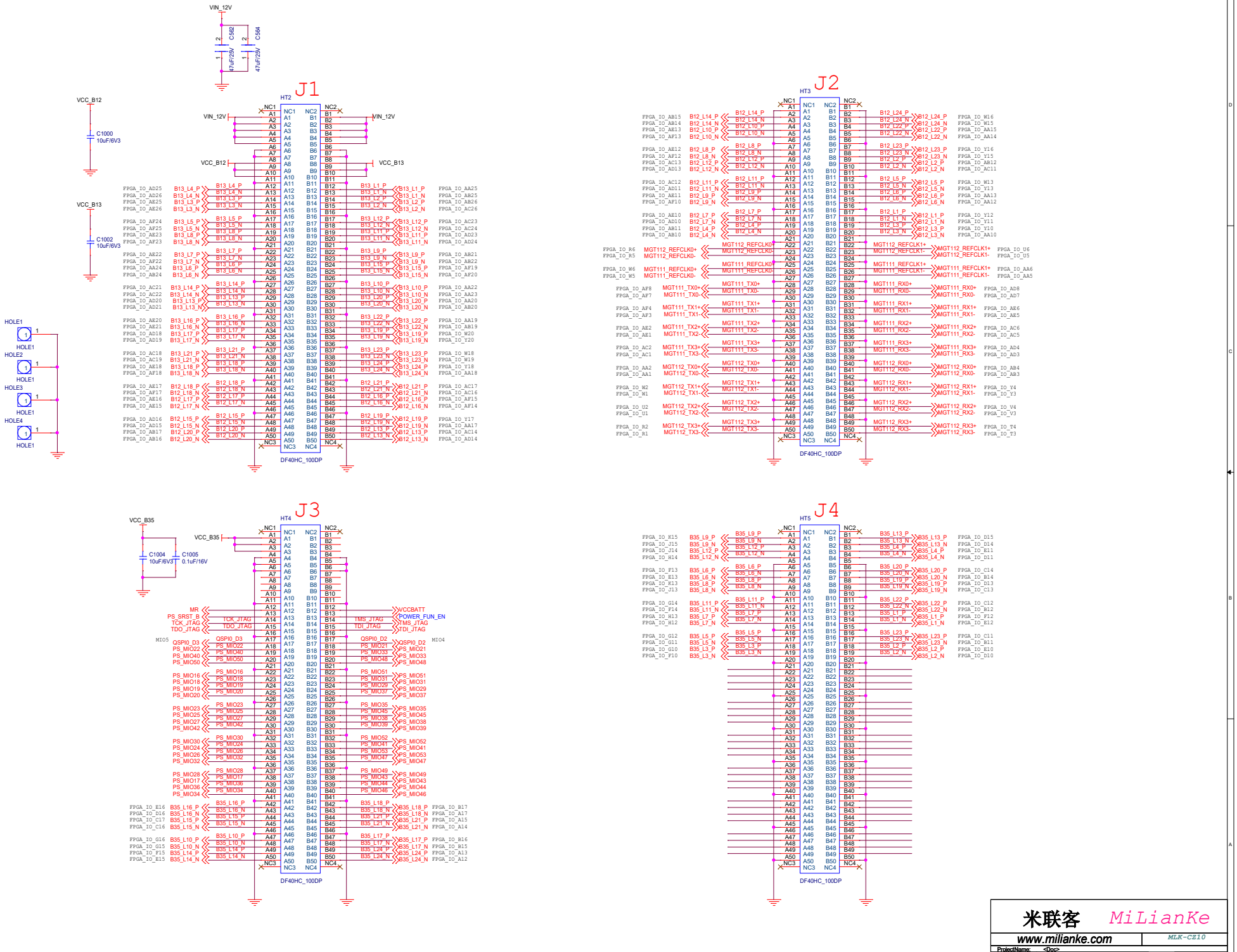
J1
J2
J3
J4
VIN_12V
VCC_B12
VCC_B13
VCC_B35
C562
C564
C1000
C1002
C1004
C1005
47uF/25V
10uF/6V3
0.1uF/16V
HOLE1
HOLE2
HOLE3
HOLE4
HT2
HT3
HT4
HT5
DF40HC_100DP
MR
PS_SRST_B
TCK_JTAG
TDO_JTAG
TMS_JTAG
TDI_JTAG
VCCBATT
POWER_FUN_EN
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